



FIG. 1  
(PRIOR ART)

FIG. 2 is a block diagram of a ranging CAM array 101 according to one embodiment of the present invention.

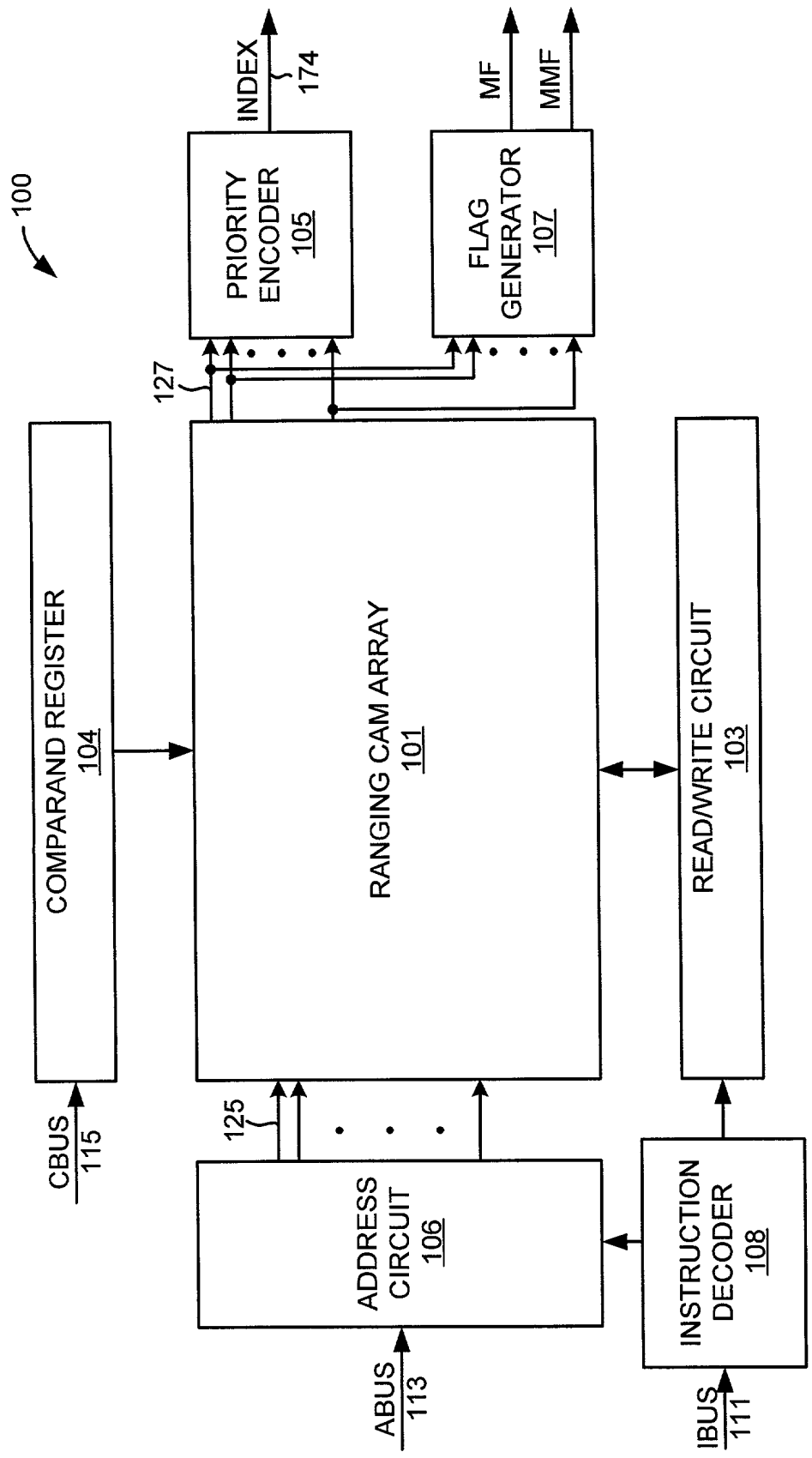


FIG. 2

FIG. 3 is a schematic diagram of a memory array structure in accordance with the present invention.

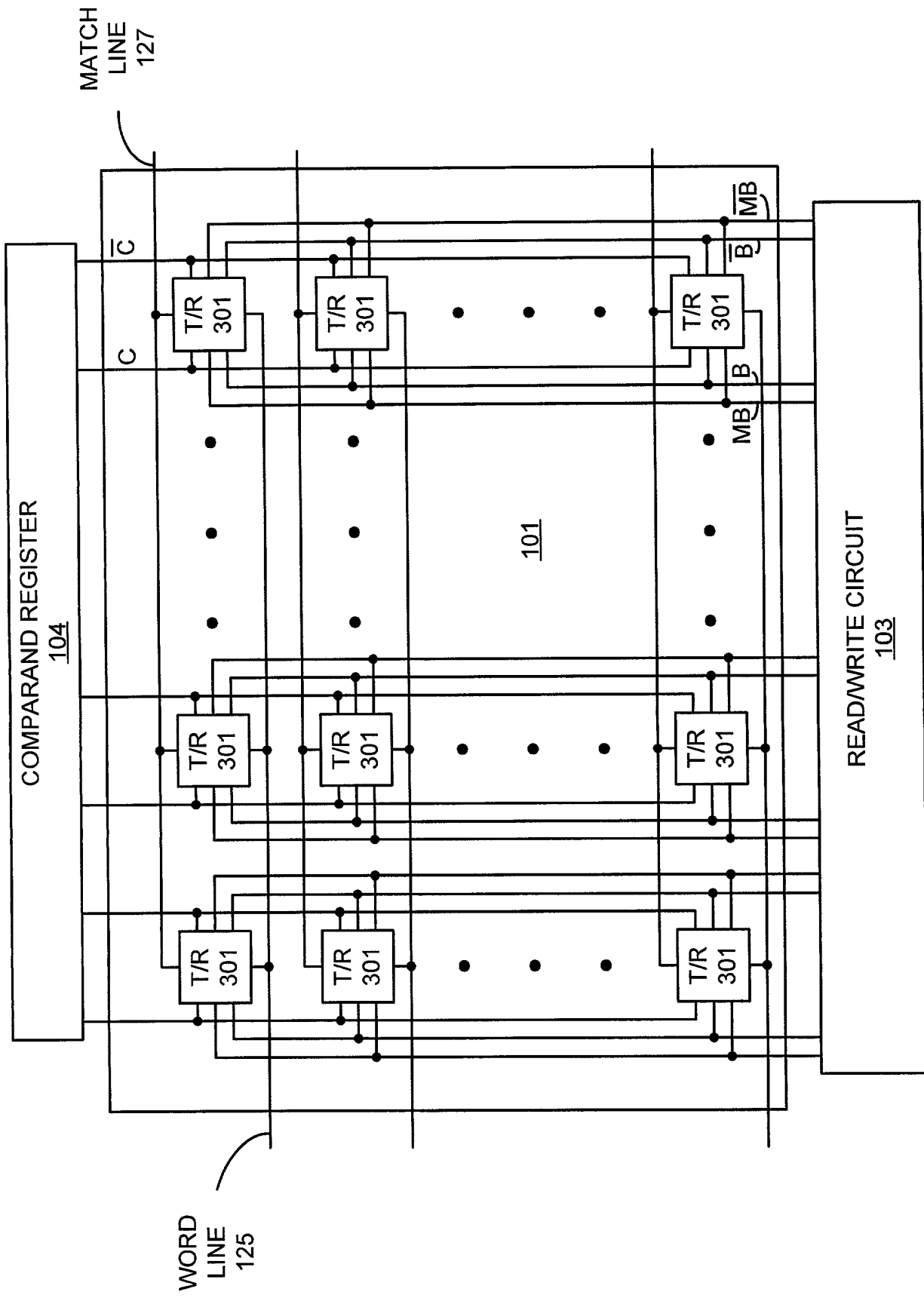


FIG. 3

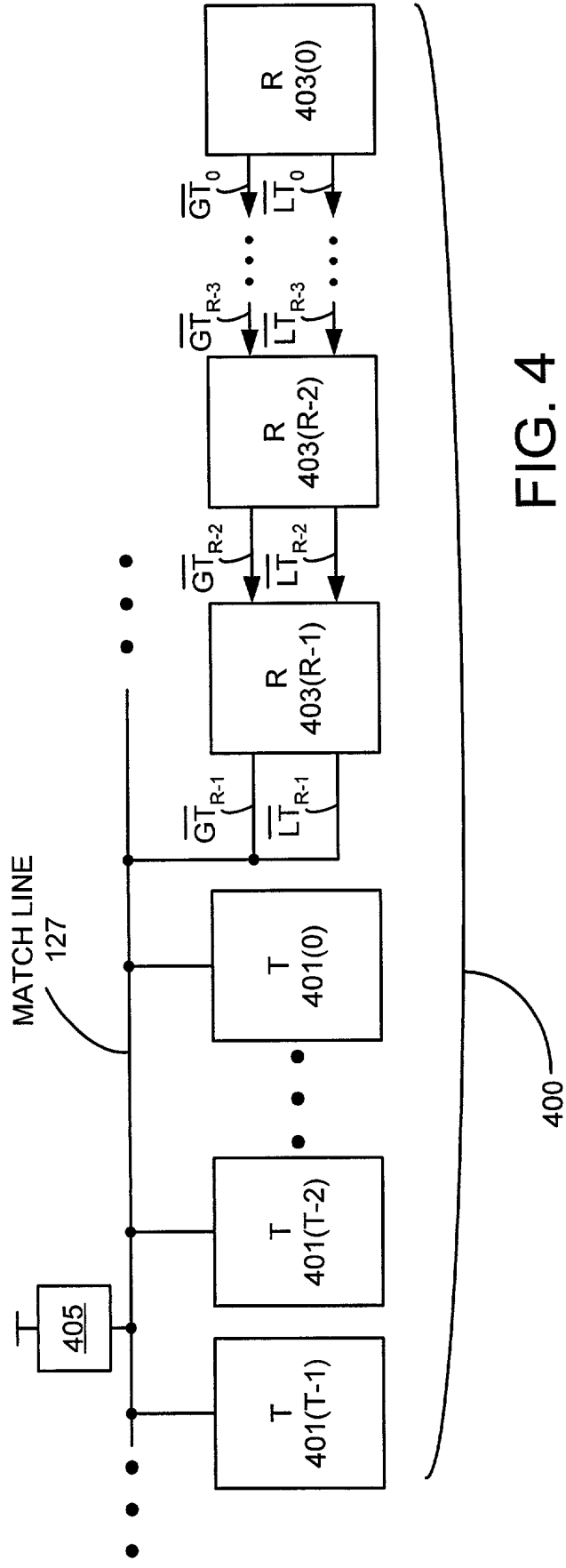


FIG. 4

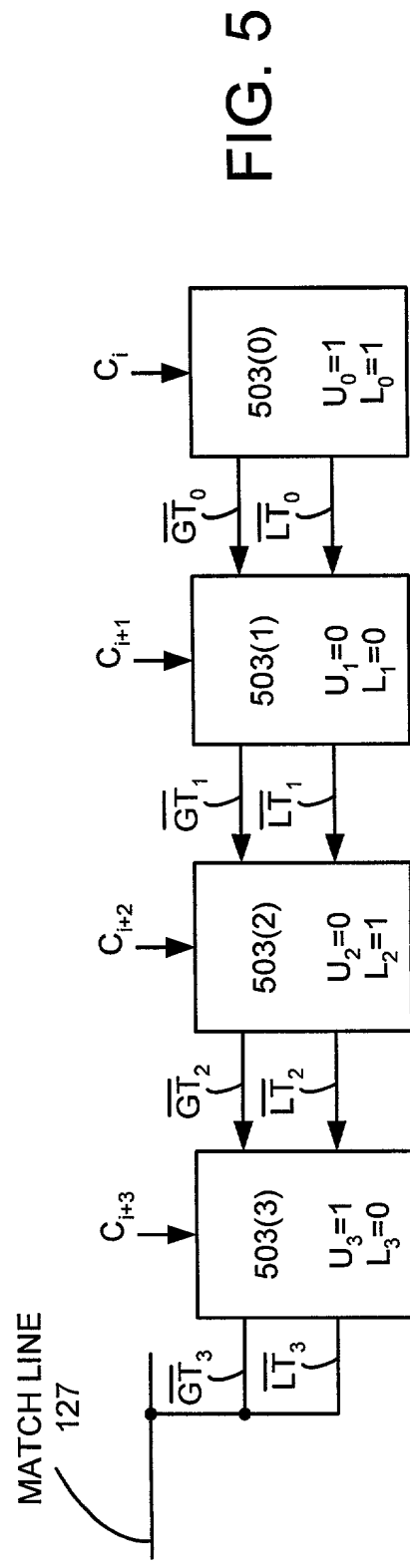


FIG. 5

MATCH LINE 127

FIG. 6

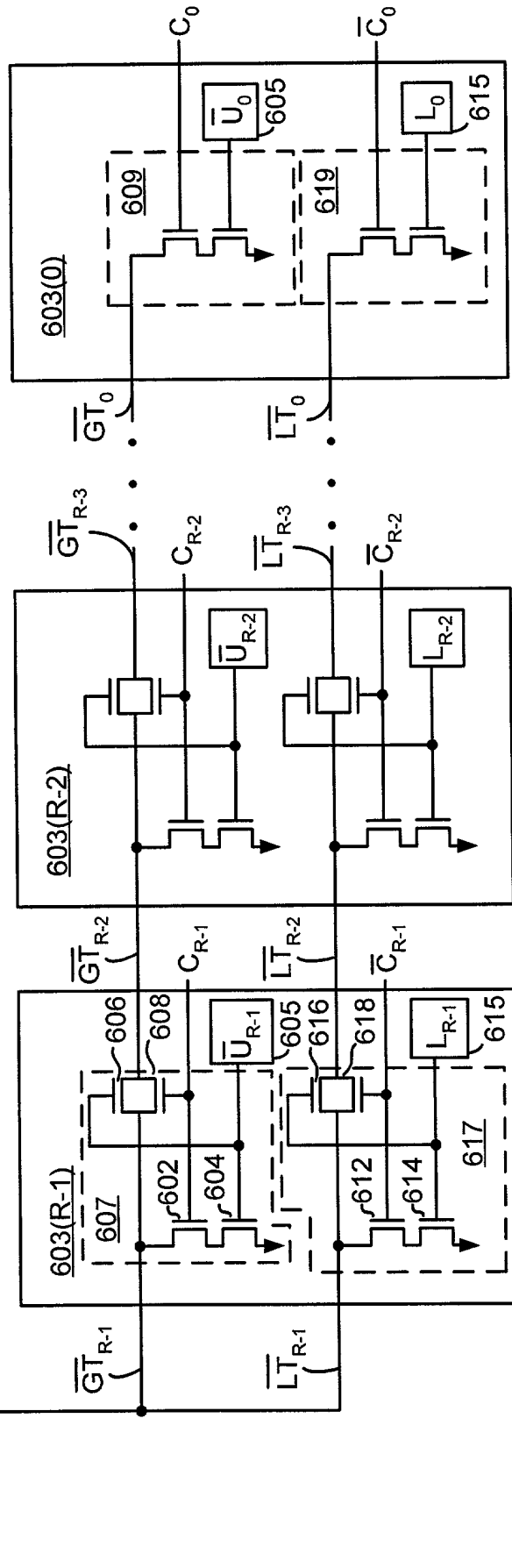


FIG. 7

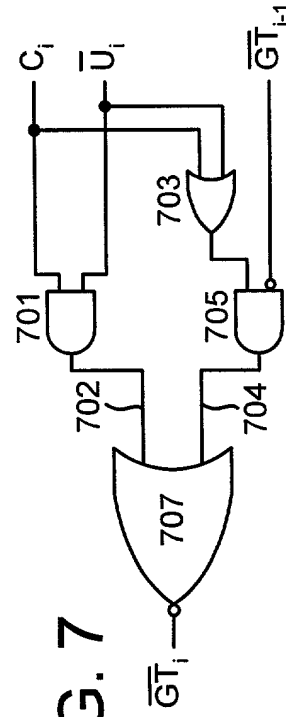
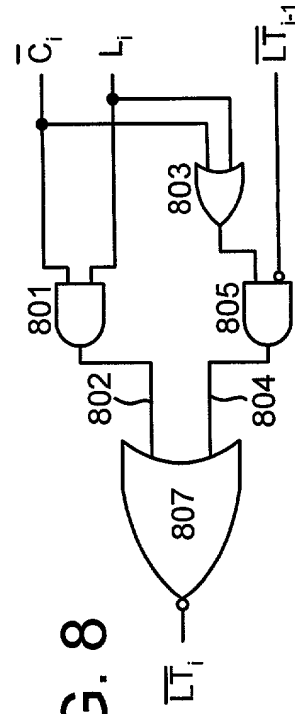


FIG. 8



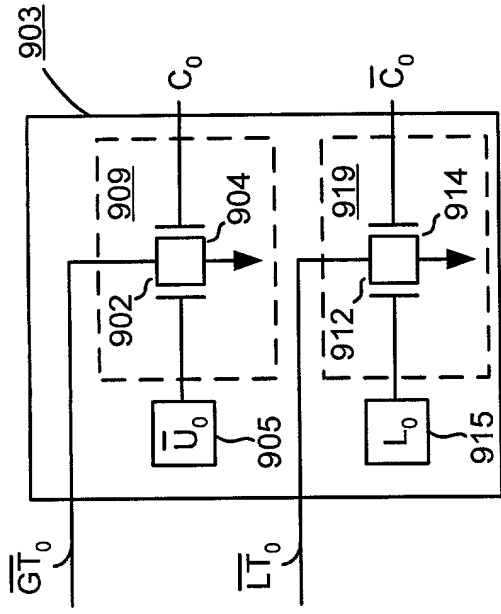


FIG. 9

FIG. 10

CLASS 0: (SP=192.11.07.23 TO 192.11.07.46) AND (DP > 1023)

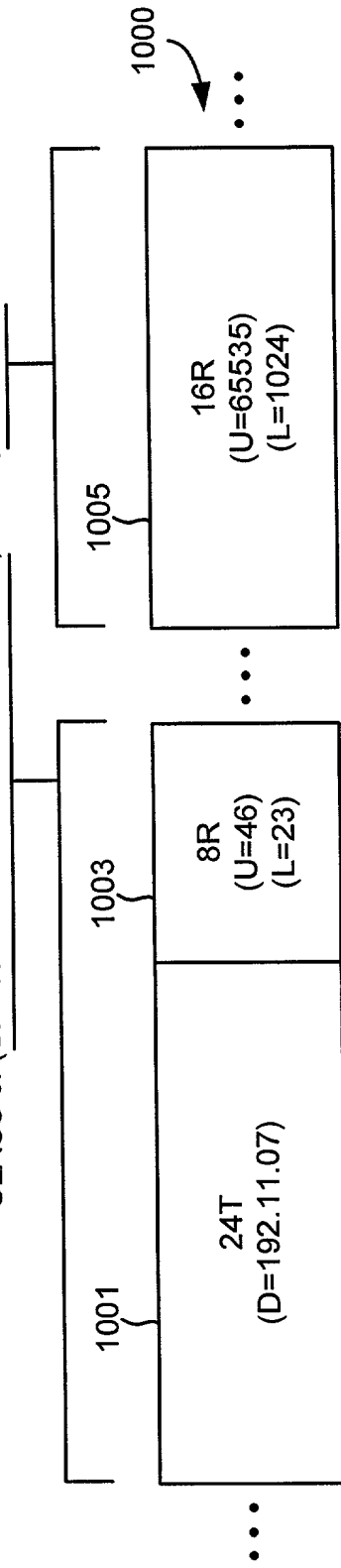
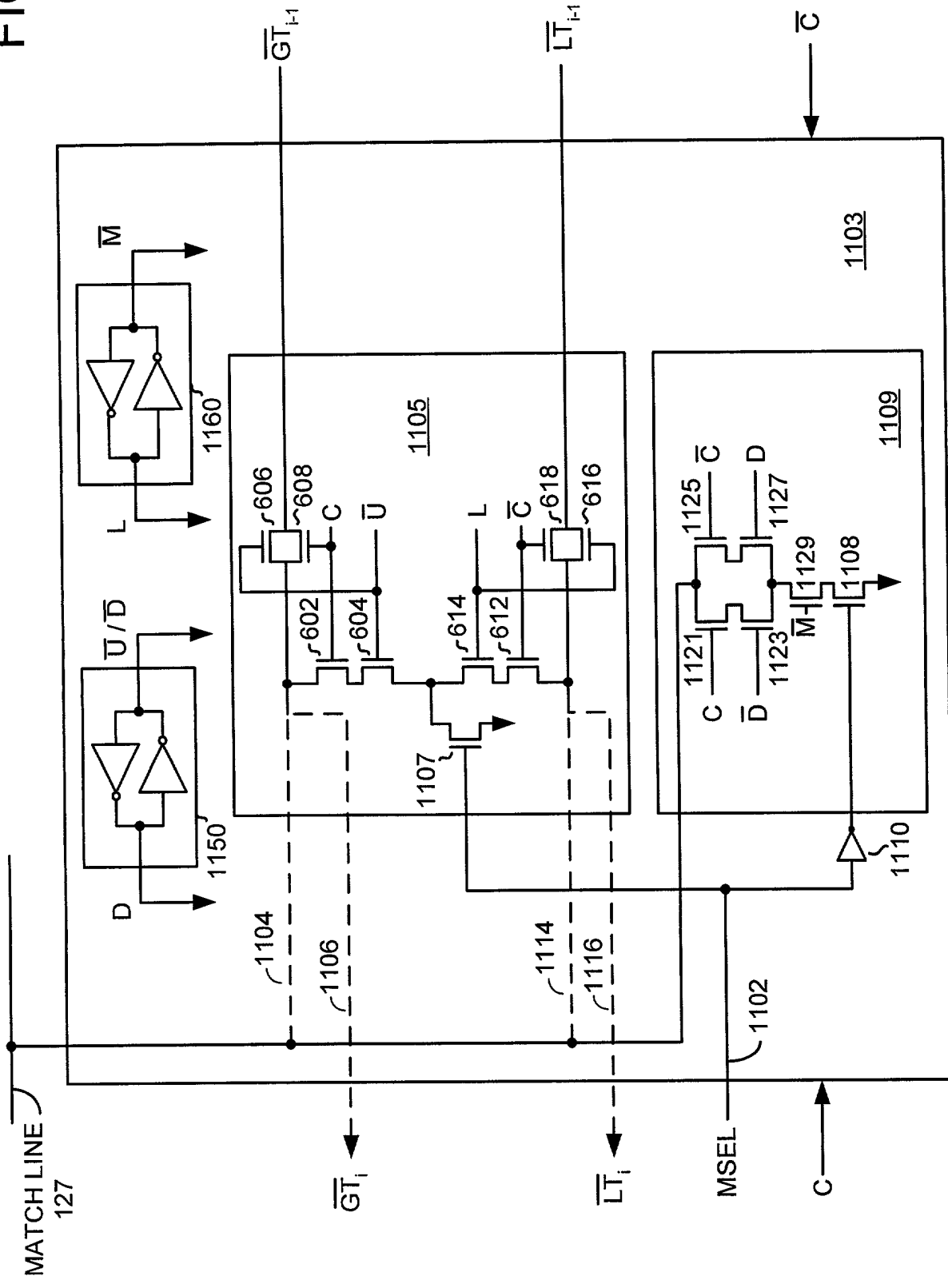


FIG. 11



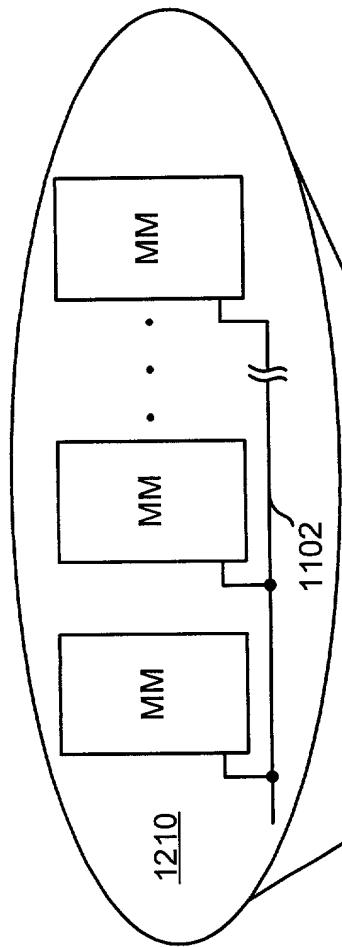
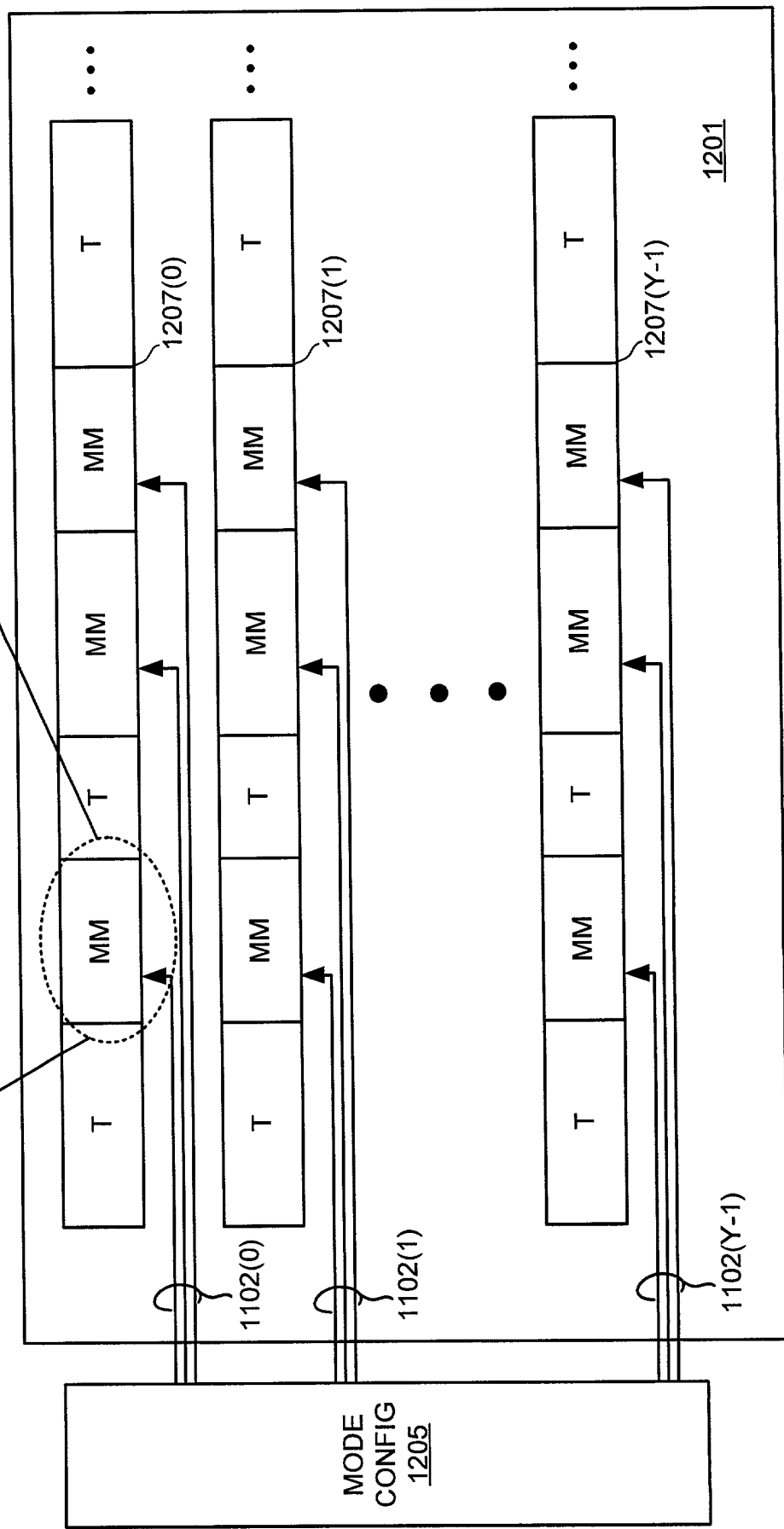


FIG. 12





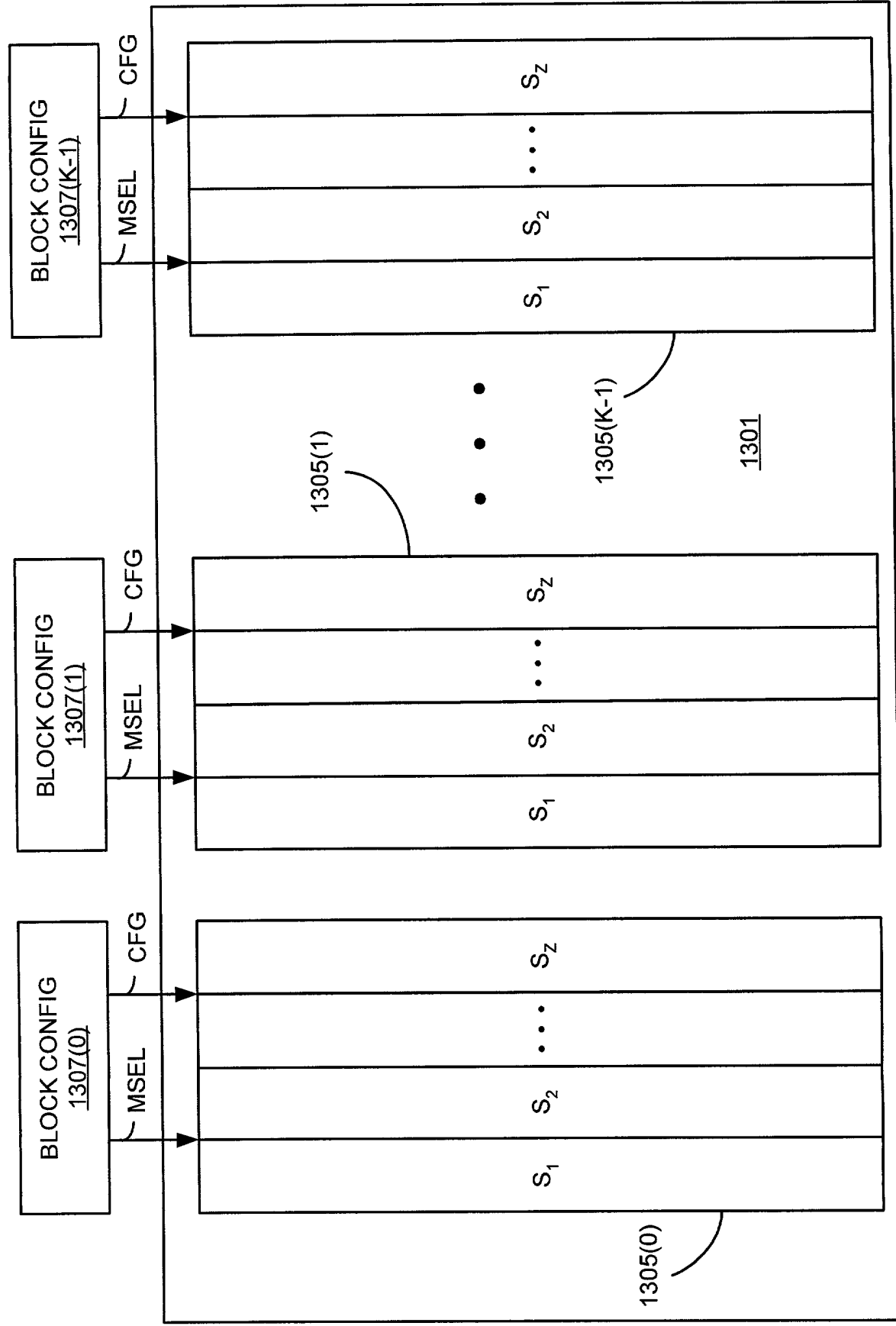
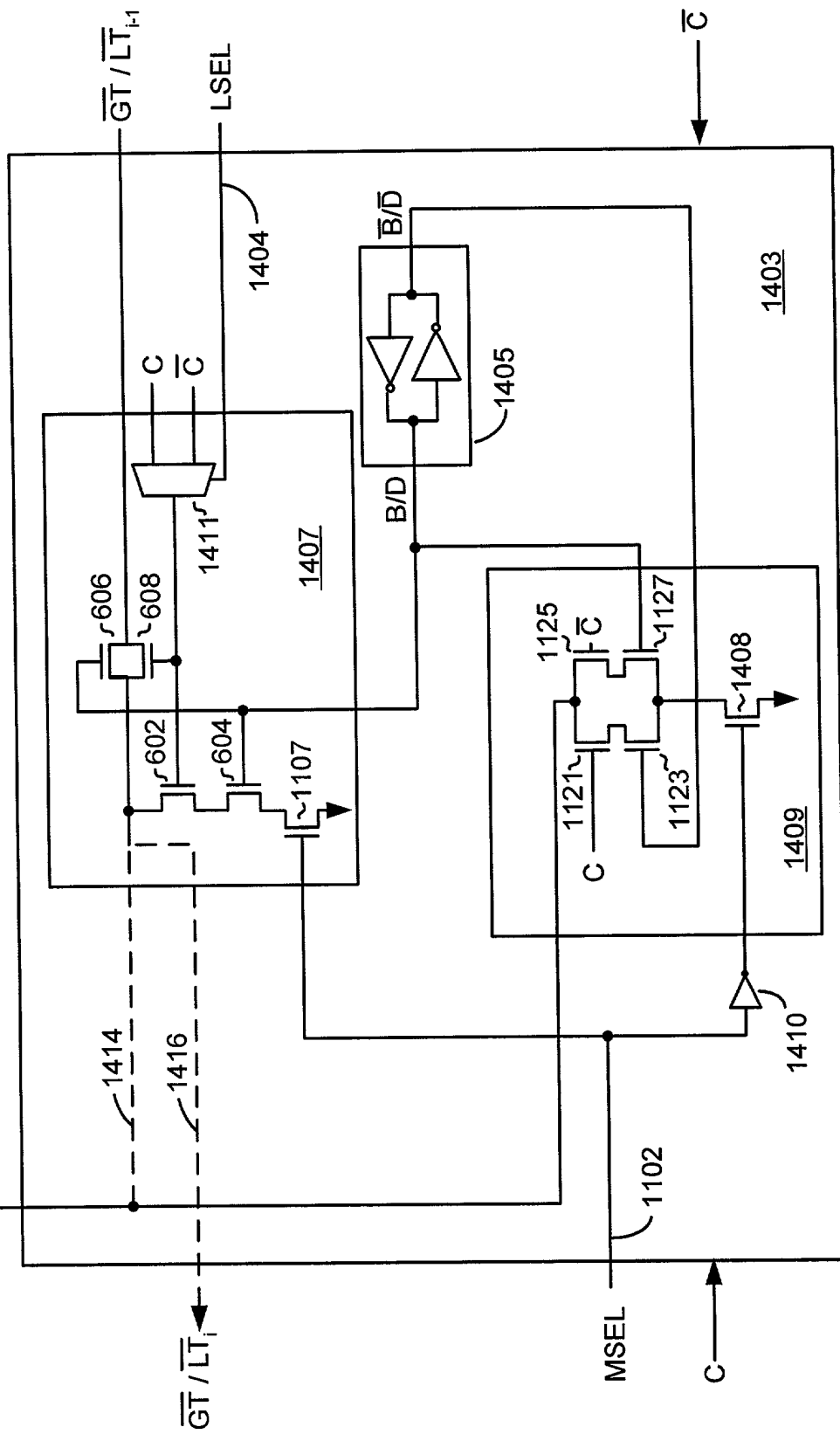


FIG. 13

FIG. 14

MATCH LINE



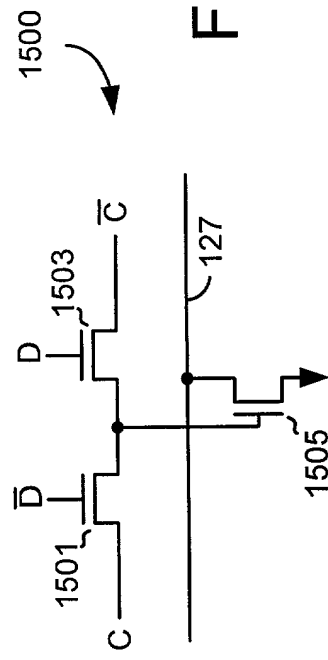
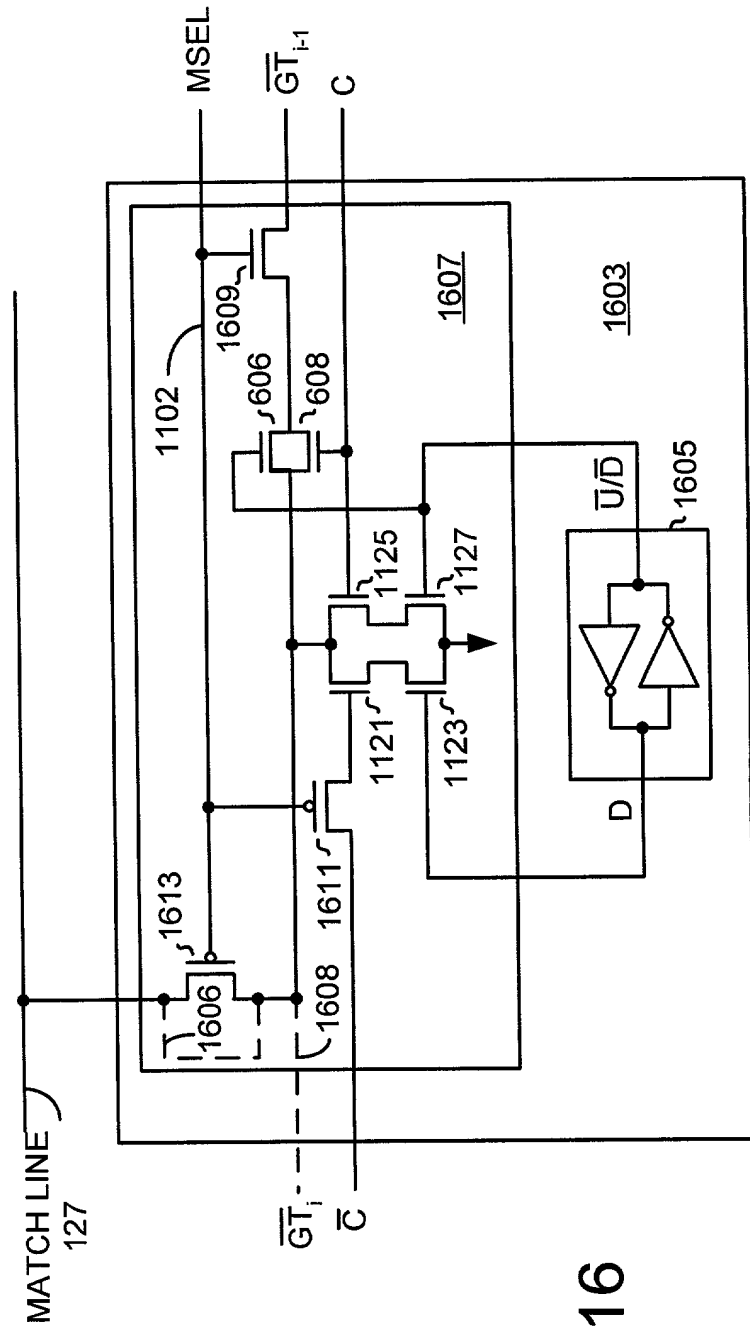


FIG. 15



**FIG. 16**

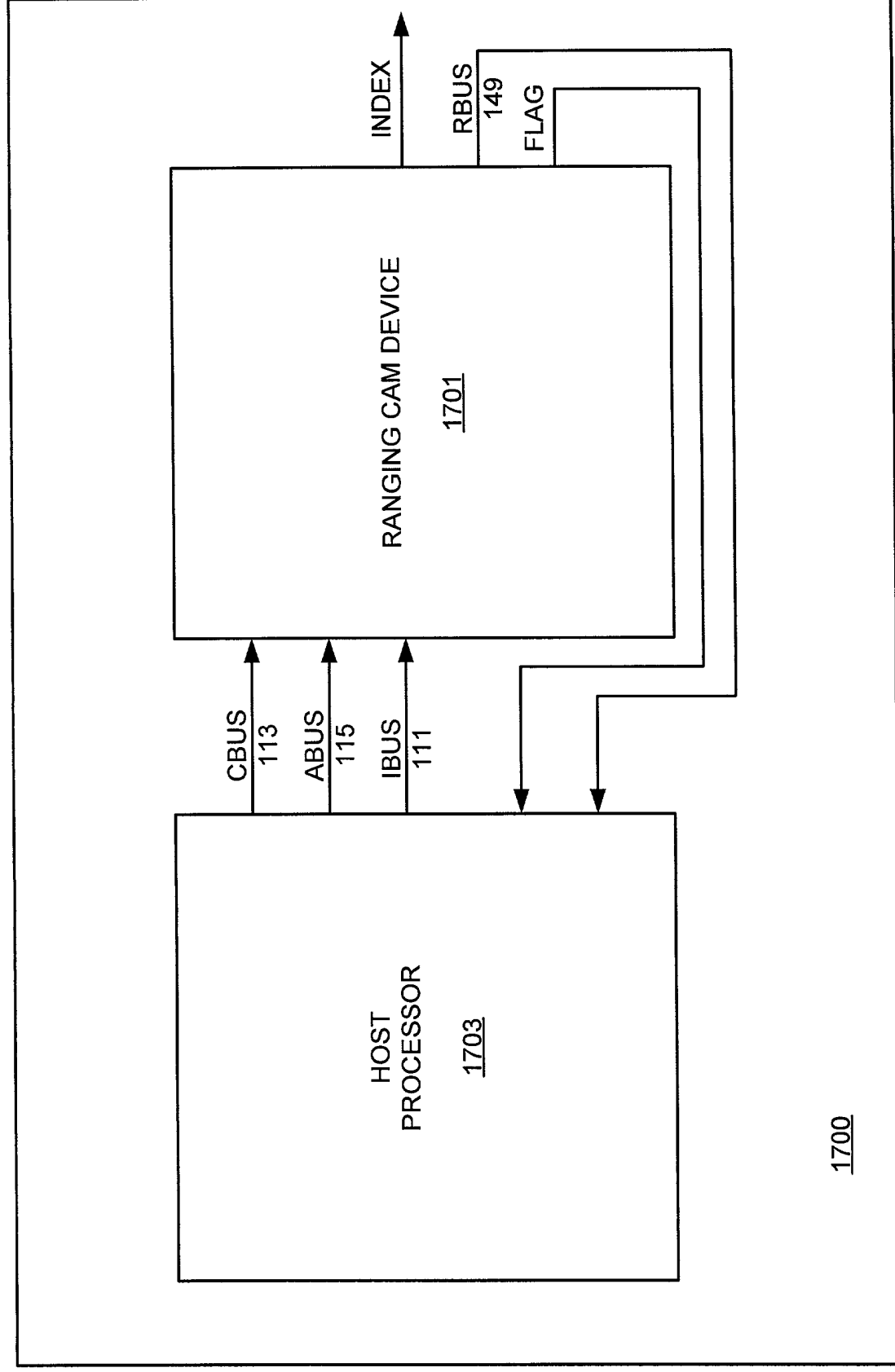


FIG. 17

